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A Solution to Harmonics Generation in Multi-Level Inverters using Carrier Based Phase Shift Pulse Width Modulation

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ABSTRACT: Multilevel inverters are suitable for high voltage & high power application due to their ability to synthesize desired output voltage with reduced total harmonic distortion (THD). This paper is focused on cascaded MLI using two unequal dc sources in order to produce a nine-level output. The proposed topology reduces the number of dc sources, switches and losses. Carrier based phase shifted PWM technique is implemented to generate switching signals and to improve the performance of output voltage in cascaded multilevel inverter (CMLI). A nine-level cascaded MLI system for 3ϕ induction motor drive is also presented in this paper. A detailed study of the technique was carried out through MATLAB/SIMULINK for THD.

KEYWORDS: Asymmetric Cascaded Multilevel Inverter (ACMLI); Switching Loss; Total Harmonic Distortion (THD).

I.INTRODUCTION

Function of a multilevel inverter is to synthesize a desired staircase output waveform from several levels of dc input voltages that can be batteries, fuel cells, etc [1].The topologies of multilevel inverter have several advantages such as lower total harmonic distortion (THD), good electromagnetic compatibility, low switching losses, high capability to operate at high voltage and lower voltage stress on semiconductor device [2]. There are three topologies for multilevel inverters: Diode- clamped, flying capacitor and cascaded H-bridge [1]. The proposed topology is the cascaded H-bridge inverter which significantly reduces the switches and the harmonic content as the number of voltage levels increases. It requires two unequal dc sources for producing a nine-level output [2]. Normally, each phase of a cascaded multilevel inverter requires "n" dc sources for 2n+1 level. The cascaded MLI is favorable for high power applications due to its modular structure, because it does not require extra clamping diodes and/or voltage balancing capacitors, and the problem of voltage unbalance is eliminated by reducing the number of dc sources [17].

Multilevel inverters are commonly modulated by using carrier based pulse width modulation techniques such as carrier based phase-shifted modulation and carrier based level-shifted modulation. Among them Carrier based Phase shift PWM (PS-PWM) have been proposed in order to reduce the harmonics at the output and to enhance the performance of the inverter. Carrier based Pulse Width Modulation (CPWM) works with a constant carrier frequency not synchronized with fundamental stator frequency which gives an optimal utilization of switching frequency. However, carrier based level-shifted modulation technique produces the best harmonic performance than the carrier based phase-shifted modulation technique [10,13]. But it is having apparent disadvantages of unequal device switching frequency and unequal device conduction periods. This is undesirable for high power applications. So the proposed method has the following advantages of equal device switching frequency and even power distribution, which is suitable for high power application [11].

The proposed strategy is employed for MLI feeding a 3ϕ Induction motor drive. Using this technique three-phase voltage has been obtained from a nine-level cascade inverter. This voltage is applied to an induction motor which ensures a high quality torque by efficiently canceling the harmonics generated by the inverter [3, 9]. Performances of

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the inverter were evaluated by observing the characteristics of stator current, rotor speed, torque and stator flux from the simulated Induction motor model.

II.NINE - LEVEL ASYMMETRIC CASCADED MULTILEVEL INVERTER

The nine-level cascaded multilevel inverter consists of two H-Bridges. The first H-Bridge H_1 consists of dc source $3V_{dc}$, whereas the second H-Bridge H_2 consists of dc source $1V_{dc}$ as shown in Fig.1. Each dc source is connected to a three phase inverter. Each inverter level can generate three different voltage outputs, $+V_{dc}$, 0, and $–V_{dc}$ by different combinations of the four switches S_1, S_2 , $S_3$and S_4. When S_1 and S_4 are on, the output is V_{dc}, when S_2 and $S_3$are on, the output is $–V_{dc}$, when either pair S_1 and S_2 or $S_3$and S_4 are on, the output is 0 [5]. The output voltage H_1 can be made equal to $-3V_{dc}$, 0, or $3V_{dc}$, while similarly the output voltage of H_2 can be made equal to $-V_{dc}$, 0, or V_{dc} by opening and closing its switches appropriately. Therefore, the output voltage of the inverter can have the values $-4V$dc, $-3V$dc, $-2V$dc, $-V$dc, 0, $4V$dc, $3V$dc, $2V$dc, Vdc, can be designed, as shown in Fig. 4. The output voltage of the first H-bridge is denoted byV_1 and the second H-bridge is denoted by V_2. The output voltage is $V=V_1+V_2$ [1]. Figs. 2–4 show the individual bridge outputs and final nine-level output. Table-I shows the conduction sequence of each switch in asymmetric nine-level inverter. Fig.1 shows the Cascaded MLI with unequal dc sources.

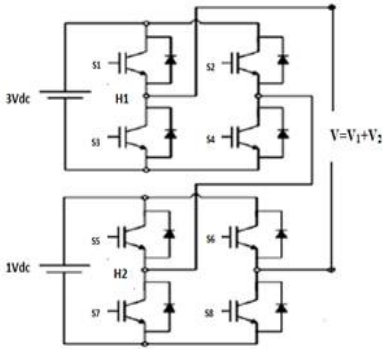

Fig.1. Cascaded MLI with unequal dc sources

Fig.2 shows the Output voltage for First bridge of MLI and fig 3 shows the output voltage of the Second bridge of MLI. Fig.4 shows the Output voltage of Nine-level Asymmetric MLI.

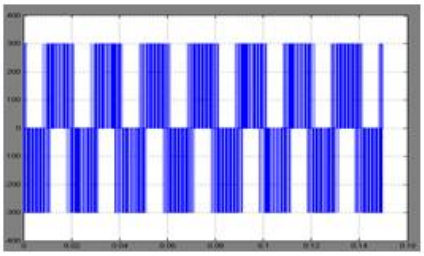

Fig 2. Output voltage of the First Bridge of MLI.

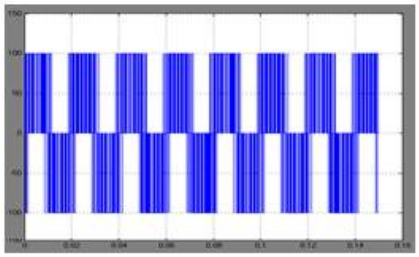

Fig3. Output voltage of the Second bridge of MLI

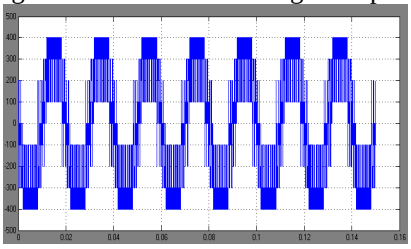

Fig. 4. Output Voltage waveform of Nine-level Asymmetric MLI.

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TABLE I. Switching States Of Cascaded MLI

Voltage	S1	S2	S3	S4	S5	S6	S7	S8
4Vdc	On	Off	Off	On	On	Off	Off	On
3Vdc	On	Off	Off	On	On	On	Off	Off
2Vdc	On	Off	Off	On	Off	On	On	Off
1Vdc	On	On	Off	Off	On	Off	Off	On
-1Vdc	Off	Off	On	On	Off	On	On	Off
-2Vdc	Off	On	On	Off	On	Off	Off	On
-3Vdc	Off	On	On	Off	Off	Off	On	On
-4Vdc	Off	On	On	Off	Off	On	On	Off

III. CARRIER BASED PHASE SHIFT PWM TECHNIQUE

Reduction of harmonics strongly depends on the inverter performance with any modulation strategy. The multicarrier sinusoidal pulse width modulation employs N-1 carriers for producing N level output. The modulation control strategies that are proposed under Multicarrier sinusoidal pulse width modulations are carrier phase disposition method and carrier phase shift modulation. The carrier phase shift modulation technique is preferred because the stresses on the switches are equally distributed compared to carrier phase disposition method particularly in producing the upper and lower levels [6-8].

The width of each pulse is varied in proportion to the amplitude of a sine wave evaluated at the centre of the same pulse. The gating signals are generated by comparing a sinusoidal reference signal with a triangular carrier wave of frequency fc. The frequency of reference signals fr, determines the inverter output frequency and its peak amplitude Ar, controls the modulation index M, and rms output voltage Vo. The number of pulses per half cycle depends on carrier frequency [10]. The phase-shift PWM modulation technique have been used to generate a phase-voltage with *m* levels, this strategy uses (*m–1*) carriers with the same amplitude, but sinusoidal reference signal is phase shifted with 120º among themselves [13]. Therefore, for a nine-level inverter, this strategy uses eight carriers. The reference and carrier waveforms for phase shift PWM technique is shown in Fig.5.Fig.5 shows the Phase shifted carrier pulse width modulation.

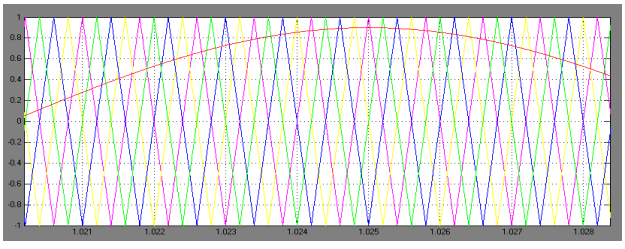

Fig. 5. Phase shifted carrier pulse width modulation

IV. SIMULATION RESULTS

To verify the proposed schemes, a simulation model for a three phase nine level cascaded MLI with induction motor load is implemented. The simulation parameters are shown in Table II. MATLAB/SIMULINK circuit for the three-phase asymmetric MLI is shown in Fig.6.

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TABLE II. MOTOR SPECIFICATIONS

S.no	Parameters	Values
1.	Ratings	4 KW, 400V, 50 Hz, 1430 rpm.
2.	Stator resistance(Rs)	1.405 Ω
3.	Rotor resistance(Rr)	1.395 Ω
4.	Inductance	Ls=0.0058 H, Lm=0.1722 H.
5.	Moment of Interia	0.0131 J
6.	Friction factor	F=0.002985
7.	Pole pairs	2
8	Main DC source voltage (Vdc)	300 V
9	Modulation Index (ma)	0.9
10	Carrier Frequency	5000 Hz
11	Rated Output Frequency	50 Hz

Fig.6 shows the Simulation circuit for asymmetric cascaded MLI.

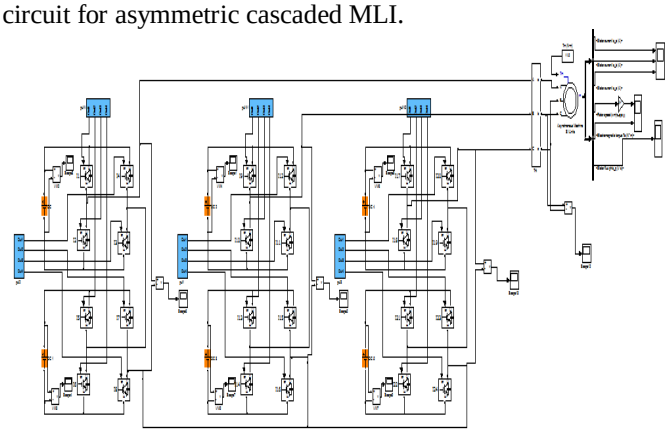

Fig 6. Carrier based Phase shifted three phase nine level Cascaded MLI

Fig.7 shows the phase voltage of asymmetric cascaded MLI and Fig.8 show the line-line voltage for asymmetric cascaded MLI.

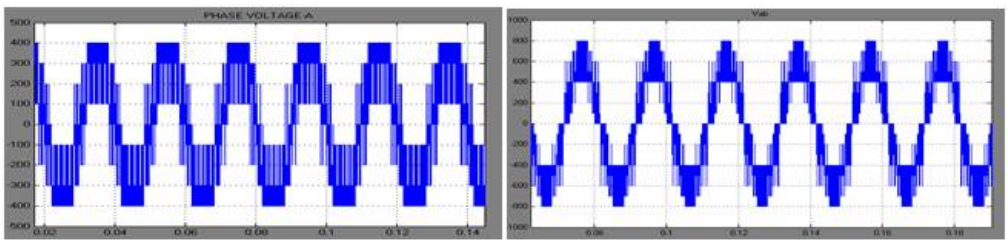

Fig. 7. Phase Voltage of Cascaded MLIFig.8 show the line-line voltage for asymmetric cascaded MLI.

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Fig.9 shows the Stator current for 3ϕ Induction motor.

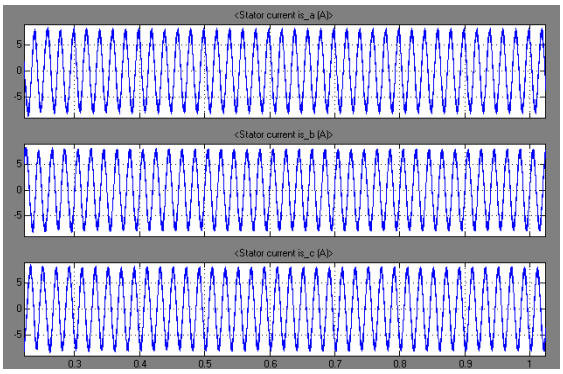

Fig. 9. Stator current of 3ϕ Induction motor.

Fig.10 shows the Rotor speed & Electromagnetic Torque for 3ϕ Induction motor. The rotor speed is always less than synchronous speed. Therefore this machines is called as Asynchronous machine. The starting torque of aninduction motor can be increased by increasing the resistance of the rotor circuit [9].Fig.11 shows the Stator flux for 3ϕ Induction motor.

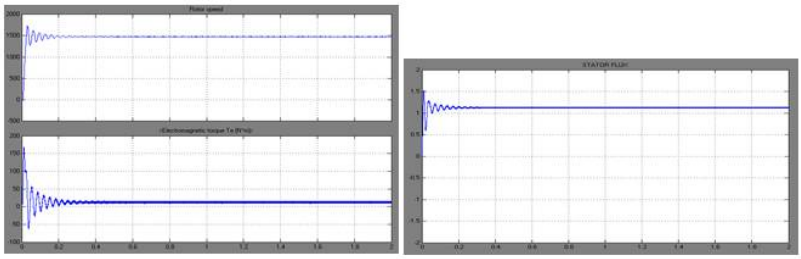

Fig.10. Rotor speed & Torque of 3ϕ Induction motor.Fig.11. Stator flux of 3ϕ Induction motor

V. TOTAL HARMONICS DISTORTION (THD) ANALYSIS

Cascaded MLI typically use IGBT switches which have low block voltage and high switching frequency [17]. Carrier-based PWM is highly conventional technique is based on the comparison of a sinusoidal reference with carrier signals which are usually selected triangular and modified in phase or vertical positions to reduce the output voltage harmonic content [12-16]. The harmonics in induction motor sometimes exhibit to run stably at speeds as low as 1/7 of their synchronous speed. This is avoided by reducing the harmonics which is shown in Figs. 13 – 15.Fig.12 shows the FFT analysis of phase voltage.Fig.13 shows the FFT analysis of Line-Line voltage.

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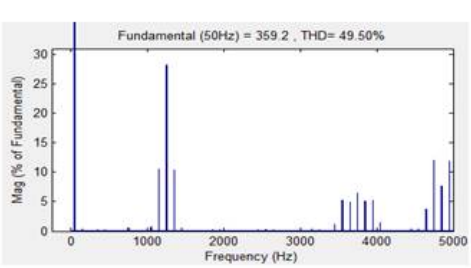

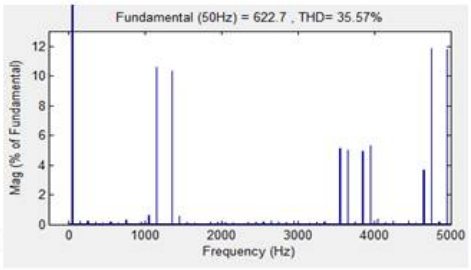

Fig.12. FFT analysis of Phase voltageFig.13. FFT analysis of Line-Line voltage

Fig.14 shows the FFT analysis of stator current.

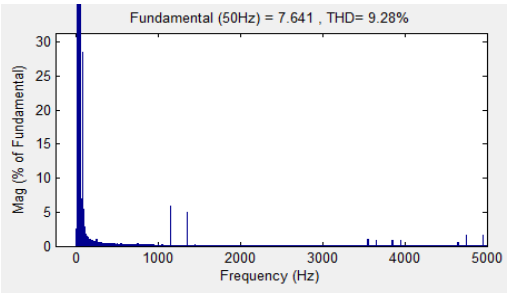

Fig.14. FFT analysis of Stator current

VI. CONCLUSION

This paper has investigated a three-phase asymmetric nine-level cascaded multilevel inverter with minimum number of switching devices thus decreasing the complexity and the cost of the circuit. By increasing the number of steps, waveform approaches the desired sinusoidal shape and THD is reduced so that less stress on the motor windings. A phase shift PWM technique has been employed and the performance of the inverter with induction motor load has been studied. From the simulation results, it is observed that the proposed technique reduces THD and balances the switching action among the switches in MLI. Particularly, FFT spectrum shows the lower order harmonics are reduced with PSPWM technique, thereby contributing to lesser torque ripples. The proposed MLI with reduced number of switches can be employed for electric vehicle applications.

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